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EXAMINER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/799,239	BROWN ET AL.
	Examiner	Art Unit	
	BEN H. LIU	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

Status

1) ☒ Responsive to communication(s) filed on <u>May 19th, 2009</u>.

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-22</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1-22</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1.   This office action is in response to an amendment/response filed on May 19th, 2009.

2.   Claims 1 and 17-19 have been amended.

3.   No claims have been cancelled.

4.   No claims have been added.

5.   Claims 1-22 are currently pending.

Claim Rejections - 35 USC § 103

6.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

7.   The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459

(1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

       1.   Determining the scope and contents of the prior art.
       2.   Ascertaining the differences between the prior art and the claims at issue.
       3.   Resolving the level of ordinary skill in the pertinent art.
       4.   Considering objective evidence present in the application indicating obviousness
             or nonobviousness.

8.   This application currently names joint inventors. In considering patentability of the

claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c)

and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9.   Claims 1, 3, 5, 7-17, 19, 21, and 22 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Amit (U.S. Patent 7,197,045) in view of Stark et al. (U.S. Patent 6,963,535).

     For claim 1, Amit discloses a processor comprising at least a portion of a first split

transmit and receive media access controller, the split transmit and receive media access

controller having a transmit unit and a receive unit physically separated from one another *(see

column 2 lines 28-33, which recite separated MAC receivers and transmitters)*; wherein the

processor comprises an interface for directing signals between the transmit unit and the receive

unit of the first split transmit and receive media access controller *(column 5 lines 1-14, which

recite a CPU 230 that directs packets between receivers and transmitters)*,

     wherein the first and second split transmit and receive media access controllers have

respective distinct addresses encoded by particular values of information bits sent over the

interface and the processor decodes said information bits so as to distinguish a first signal sent

between the transmit and receive units of the first split transmit and receive media access

controller from a second signal sent between the transmit and receive units of the second split

transmit and receive media access controller *(see column 5 lines 1-14, which recite CPU 230 that utilizes information bits to distinguish signals belonging a first and second transmitter and a second information bit to distinguish signals belonging a first and second receiver; since each transmitter and receiver is identified by a unique bit value, each transmit and receive controller can be uniquely identified by specifying the corresponding receiver and transmitter).*

Amit discloses all the subject matter of the claimed invention with the exception wherein signals from a first split transmit and receive media access controller are multiplexed with signals directed between a transmit unit and a receive unit of at least a second split transmit and receive media access controller. Stark et al. from the same or similar fields of endeavor teach a MAC bus that provides connections between a number of MAC interfaces using a multiplexer scheme *(see abstract)*. The MAC bus uses multiplexers that include a MAC data-in bus and MAC data-out bus *(see column 3 lines 19-30)* that allows data from one MAC interface to reach another MAC interface *(see figure 3)*. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the MAC bus that provides connections between a number of MAC interfaces as taught by Stark et al. with the MAC interface that provides separate transmit and receive units as taught by Amit. The MAC bus and multiplexers as taught by Stark et al. can be coupled between the switch interface 352 and each of the receive 336 or transmit 334 MAC interfaces as taught by Amit to provide an interface that is configured to multiplex signals between the transmit unit and the receive unit of the first split transmit and receive media access controller with signals directed between a transmit unit and a receive unit of at least a second split transmit and receive media access controller. The motivation for using the MAC bus interface with the MAC interface that includes separated transmit and receive units

is to improve the compatibility of the MAC communication bus with a variety of MAC

interfaces.

      For claims 3, 21 and 22, Amit discloses a processor comprising a split transmit and

receive media access controller having a transmit unit and a receive unit physically separated

from one another wherein one or more of the transmit units are implemented on a first integrated

circuit and one or more of the receive units are implemented on a second integrated circuit *(see*

column 2 lines 34-42).

      For claim 5, Amit discloses a processor comprising a split transmit and receive media

access controller having a transmit unit and a receive unit physically separated from one another

(see column 2 lines 28-33, which recite separated MAC receivers and transmitters). Amit

discloses all the subject matter of the claimed invention with the exception wherein an interface

comprises a receive interface block coupled to a generate interface block via an interface bus, the

generate interface block receiving signals from a plurality of media access controller receive

units and multiplexing the signals onto the interface bus for delivery to the receive interface

block, the receive interface block demultiplexing the signals from the interface bus for delivery

to appropriates ones of a plurality of media access controller transmit units. Stark et al. from the

same or similar fields of endeavor teach a MAC bus that provides connections between a number

of MAC interfaces using a multiplexer scheme *(see abstract)*. The MAC bus uses multiplexers

that include a MAC data-in bus (a generate interface block) and MAC data-out bus (a receive

interface block) *(see column 3 lines 19-30)* that allows data from one MAC interface to reach

another MAC interface *(see figure 3)*. Thus, it would have been obvious to the person of

ordinary skill in the art at the time of the invention to use the MAC bus that provides connections

between a number of MAC interfaces as taught by Stark et al. with the MAC interface that

provides separate transmit and receive units as taught by Amit. The MAC bus can be

implemented by coupling the MAC bus as taught by Stark et al. between the CPU and switch

interface of the MAC interface that includes separated transmit and receive units as taught by

Amit. The motivation for using the MAC bus interface with the MAC interface that includes

separated transmit and receive units is to improve the compatibility of the MAC communication

bus with a variety of MAC interfaces.

      For claim 7, Amit discloses all the subject matter of the claimed invention with the

exception wherein the interface bus comprises a five-bit wide information signal bus and at least

one clock signal line. Stark et al. from the same or similar fields of endeavor teach a MAC bus

that provides connections between a number of MAC interfaces using a multiplexer scheme *(see*

abstract). The MAC includes a 32 bit information signal bus *(see figures 4-5, which recite*

signal buses 34 and 46) as well as a clock signal *(see column 8 lines 28-35 and figures 19-22,*

which recite a clocking signal that controls the buses). The information bus as taught by Stark et

al. is 32 bits wide but is a design choice that may be modified according to the complexity and

desired performance of the bus system. Thus, it would have been obvious to the person of

ordinary skill in the art at the time of the invention to use the MAC bus that provides connections

between a number of MAC interfaces using an information bus and clocking signal as taught by

Stark et al. with the MAC interface that provides separate transmit and receive units as taught by

Amit. The MAC bus can be implemented by coupling the MAC bus as taught by Stark et al.

between the CPU and switch interface of the MAC interface that includes separated transmit and

receive units as taught by Amit. The motivation for using the MAC bus interface with the MAC

interface that includes separated transmit and receive units is to improve the compatibility of the

MAC communication bus with a variety of MAC interfaces.

For claim 8, Amit discloses a processor comprising a split transmit and receive media

access controller having a transmit unit and a receive unit physically separated from one another

wherein the interface bus comprises a separate dedicated information signal bus for delivering

carrier sense signals between one or more of the receive units and one or more of the transmit

units in an internal mode of operation of the interface *(see column 5 lines 20-27, which recite an*

Ethernet switch interface 352 wherein the Ethernet protocol employs carrier sense multiple

access to deliver a carrier signal to indicate impending transmission).

For claim 9, Amit discloses a processor comprising a split transmit and receive media

access controller having a transmit unit and a receive unit physically separated from one another

wherein the signals received by the generate interface block for delivery to the receive interface

block comprise one or more of carrier sense signals, auto-negotiation signals, flow control

signals, and deference reset signals *(see column 5 lines 20-27, which recite an Ethernet switch*

interface 352 wherein the Ethernet protocol employs carrier sense multiple access to deliver a

carrier signal to indicate impending transmission).

For claim 10, Amit discloses a processor comprising a split transmit and receive media

access controller having a transmit unit and a receive unit physically separated from one another

wherein the signals received by the generate interface block are multiplexed onto the interface

bus using a priority-based selection mechanism which assigns the highest priority to the carrier

sense signals, the second highest priority to the auto-negotiation signals, and lower priorities to

the flow control and deference reset signals *(see column 6 lines 10-14, which recite a priority queue for different types of signals)*.

For claim 11, Amit discloses all the subject matter of the claimed invention with the exception wherein the interface operates in accordance with a state machine having at least a synchronization state, a control address state and one or more data states. Stark et al. from the same or similar fields of endeavor teach a MAC bus that provides connections between a number of MAC interfaces using a multiplexer scheme *(see abstract)*. The MAC bus uses state machines wherein the states control the operation of the bus with the location of the registers *(see column 9 lines 13-26 and figures 14-16)*. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the MAC bus that uses state machines as taught by Stark et al. with the MAC interface that provides separate transmit and receive units as taught by Amit The MAC bus that uses state machines can be implemented by coupling the MAC bus as taught by Stark et al. between the CPU and switch interface of the MAC interface that includes separated transmit and receive units as taught by Amit. The state machine for the bus can be implemented using registers that receive appropriate control signals as taught by Stark et al. The motivation for using the MAC bus interface with the MAC interface that uses state machines is to improve the compatibility of the MAC communication bus with a variety of MAC interfaces.

For claim 12, Amit discloses all the subject matter of the claimed invention with the exception wherein the control address state carries information regarding signal type and signal interface address. Stark et al. from the same or similar fields of endeavor teach a MAC bus that provides connections between a number of MAC interfaces using a multiplexer scheme *(see abstract)*. The MAC bus uses state machines wherein the states control the operation of the bus

with the location of the registers *(see column 9 lines 13-26 and figures 14-16)*. Thus, it would

have been obvious to the person of ordinary skill in the art at the time of the invention to use the

MAC bus that uses state machines as taught by Stark et al. with the MAC interface that provides

separate transmit and receive units as taught by Amit. The MAC bus that uses state machines

can be implemented by coupling the MAC bus as taught by Stark et al. between the CPU and

switch interface of the MAC interface that includes separated transmit and receive units as taught

by Amit. The state machine for the bus can be implemented using registers that receive

appropriate control signals as taught by Stark et al. The motivation for using the MAC bus

interface with the MAC interface that uses state machines is to improve the compatibility of the

MAC communication bus with a variety of MAC interfaces.

     For claim 13, Amit discloses a processor comprising a split transmit and receive media

access controller having a transmit unit and a receive unit physically separated from one another

wherein the interface comprises a plurality of channels, each having one or more ports associated

therewith, and wherein a given signal to be directed between transmit and receive units of a

given split transmit and receive media access controller is assigned to a particular channel and

port of the interface *(see column 6 lines 15-21, which recite adding a descriptor to designate*

which queue a packet should go).

     For claim 14, Amit discloses a processor comprising a split transmit and receive media

access controller having a transmit unit and a receive unit physically separated from one another

wherein each of the channels may have up to eight ports, with a single-bit nibble address being

utilized to identify a particular one of first and second four-port groups of a given eight-port

channel *(see column 6 lines 15-21, which recite adding a descriptor used as an address to the appropriate queue)*.

For claim 15, Amit discloses a processor comprising a split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another wherein the processor comprises an integrated circuit *(see column 2 lines 35-42, which recite a communication device that comprises a transmitter and receiver IC)*.

For claim 16, Amit discloses a processor comprising a split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another wherein the processor comprises a network processor *(see column 2 lines 43-47, which recite a communication device that comprises a CPU processor)*.

For claim 17, Amit discloses a method for use in a processor comprising at least a portion of a first split transmit and receive media access controller, the split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another *(see column 2 lines 28-33, which recite separated MAC receivers and transmitters)*, the method comprising the step of multiplexing onto a common interface signals to be directed between the transmit unit and the receive unit of the first split transmit and receive media access controller *(column 5 lines 1-14, which recite a CPU 230 that directs packets between receivers and transmitters)*,

wherein the multiplexing step further comprises the step of: associating the first and second split transmit and receive media access controllers with respective distinct addresses encoded by particular values of information bits sent over the interface; wherein said information bits are decoded so as to distinguish a first signal sent between the transmit and receive units of

the first split transmit and receive media access controller from a second signal sent between the

transmit and receive units of the second split transmit and receive media access controller *(see*

column 5 lines 1-14, which recite CPU 230 that utilizes information bits to distinguish signals

belonging a first and second transmitter and a second information bit to distinguish signals

belonging a first and second receiver; since each transmitter and receiver is identified by a

unique bit value, each transmit and receive controller can be uniquely identified by specifying

the corresponding receiver and transmitter).

      Amit discloses all the subject matter of the claimed invention with the exception wherein

the method comprises the step of multiplexing onto a common interface signals to be directed

between a transmit unit and a receive unit of at least a second split transmit and receive media

access controller. Stark et al. from the same or similar fields of endeavor teach a MAC bus that

provides connections between a number of MAC interfaces using a multiplexer scheme *(see*

abstract). The MAC bus uses multiplexers that include a MAC data-in bus and MAC data-out

bus *(see column 3 lines 19-30)* that allows data from one MAC interface to reach another MAC

interface *(see figure 3)*. Thus, it would have been obvious to the person of ordinary skill in the

art at the time of the invention to use the MAC bus that provides connections between a number

of MAC interfaces as taught by Stark et al. with the MAC interface that provides separate

transmit and receive units as taught by Amit. The MAC bus and multiplexers as taught by Stark

et al. can be coupled between the switch interface 352 and each of the receive 336 or transmit

334 MAC interfaces as taught by Amit to provide an interface that is configured to multiplex

signals between the transmit unit and the receive unit of the first split transmit and receive media

access controller with signals directed between a transmit unit and a receive unit of at least a

second split transmit and receive media access controller. The motivation for using the MAC

bus interface with the MAC interface that includes separated transmit and receive units is to

improve the compatibility of the MAC communication bus with a variety of MAC interfaces.

  For claim 19, Amit discloses an integrated circuit *(see column 2 lines 35-42, that recites*

implementing MAC units on an integrated circuit) comprising at least a portion of a first split

transmit and receive media access controller, the split transmit and receive media access

controller having a transmit unit and a receive unit physically separated from one another *(see*

column 2 lines 28-33, which recite separated MAC receivers and transmitters); wherein the

processor comprises an interface for directing signals between the transmit unit and the receive

unit of the first split transmit and receive media access controller *(column 5 lines 1-14, which*

recite a CPU 230 that directs packets between receivers and transmitters),

  wherein the first and second split transmit and receive media access controllers have

respective distinct addresses encoded by particular values of information bits sent over the

interface and said information bits are decoded in order to distinguish a first signal sent between

the transmit and receive units of the first split transmit and receive media access controller from

a second signal sent between the transmit and receive units of the second split transmit and

receive media access controller *(see column 5 lines 1-14, which recite CPU 230 that utilizes*

information bits to distinguish signals belonging a first and second transmitter and a second

information bit to distinguish signals belonging a first and second receiver; since each

transmitter and receiver is identified by a unique bit value, each transmit and receive controller

can be uniquely identified by specifying the corresponding receiver and transmitter).

Amit discloses all the subject matter of the claimed invention with the exception wherein signals from a first split transmit and receive media access controller are multiplexed with signals directed between a transmit unit and a receive unit of at least a second split transmit and receive media access controller. Stark et al. from the same or similar fields of endeavor teach a MAC bus that provides connections between a number of MAC interfaces using a multiplexer scheme *(see abstract)*. The MAC bus uses multiplexers that include a MAC data-in bus and MAC data-out bus *(see column 3 lines 19-30)* that allows data from one MAC interface to reach another MAC interface *(see figure 3)*. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the MAC bus that provides connections between a number of MAC interfaces as taught by Stark et al. with the MAC interface that provides separate transmit and receive units as taught by Amit. The MAC bus and multiplexers as taught by Stark et al. can be coupled between the switch interface 352 and each of the receive 336 or transmit 334 MAC interfaces as taught by Amit to provide an interface that is configured to multiplex signals between the transmit unit and the receive unit of the first split transmit and receive media access controller with signals directed between a transmit unit and a receive unit of at least a second split transmit and receive media access controller. The motivation for using the MAC bus interface with the MAC interface that includes separated transmit and receive units is to improve the compatibility of the MAC communication bus with a variety of MAC interfaces.

10.   Claims 2, 4, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amit

(U.S. Patent 7,197,045) in view of Stark et al. (U.S. Patent 6,963,535) as applied to claim 1 and

further in view of Bellenger (U.S. Patent 6,256,306).

      For claims 2 and 20, Amit discloses all the subject matter of the claimed invention with

the exception wherein one or more of the transmit units are implemented in a first region of an

integrated circuit, and one or more of the receive units are implemented in a second region of the

integrated circuit, remote from the first region. Bellenger from the same or similar fields of

endeavor teach a switch node including a plurality of ports with MAC units integrated on an

integrated circuit *(see column 8 lines 10-19 and figure 3)*. Thus, it would have been obvious to

the person of ordinary skill in the art at the time of the invention to use the switch node including

a plurality of ports with MAC units integrated on an integrated circuit as taught by Bellenger

with the MAC interface that provides separate transmit and receive units as taught by Amit. The

switch node including a plurality of ports with MAC units integrated on an integrated circuit can

be implemented by replacing the MAC units on the same integrated circuit as taught by

Bellenger with the MAC interface that provides separate transmit and receive units as taught by

Amit. The motivation for using the switch node including a plurality of ports with MAC units

integrated on an integrated circuit with the MAC interface that provides separate transmit and

receive units is to improve the reliability of the system by reducing inter-chip signaling and data

flow.

      For claim 4, Amit discloses all the subject matter of the claimed invention with the

exception wherein the interface is configured to deliver signals between one or more transmit

units and one or more receive units where the transmit units and the receive units are

implemented on the same integrated circuit. However, Amit discloses implementing a plurality

of transmit and receive MAC units on separate integrated circuits *(see column 2 lines 35-42)*,

thus providing an external mode of operation. Bellenger from the same or similar fields of

endeavor teach a switch node including a plurality of ports with MAC units integrated on an

integrated circuit 200 *(see column 8 lines 10-19 and figure 3)* that includes a bus 210 to deliver

signals between the MAC units *(see figure 3)*. Specifically, Bellenger teaches a switch node

including a plurality of ports with MAC units integrated on an integrated circuit *(see column 8*

lines 10-19 and figure 3) thus providing an internal mode of operation. Thus, it would have been

obvious to the person of ordinary skill in the art at the time of the invention to use the switch

node including a plurality of ports with MAC units integrated on an integrated circuit as taught

by Bellenger with the MAC interface that provides separate transmit and receive units as taught

by Amit. The switch node including a plurality of ports with MAC units integrated on an

integrated circuit can be implemented by replacing the MAC units on the same integrated circuit

as taught by Bellenger with the MAC interface that provides separate transmit and receive units

as taught by Amit. The motivation for using the switch node including a plurality of ports with

MAC units integrated on an integrated circuit with the MAC interface that provides separate

transmit and receive units is to improve the reliability of the system by reducing inter-chip

controls.

11.   Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Amit (U.S. Patent

7,197,045) in view of Stark et al. (U.S. Patent 6,963,535) as applied to claim 1 and further in

view of Appala et al. (U.S. Patent 6,862,265).

For claim 6, Amit and Stark et al. discloses all the subject matter of the claimed

invention with the exception wherein the interface block multiplexes the signals onto the

interface bus utilizing a plurality of round-robin arbiters. Appala et al. from the same or similar

fields of endeavor teach a round robin scheduler that supplies the data frames to the

corresponding transmit port *(see column 4 lines57-67, column 5 lines 1-3, and figure 2)*. Thus, it

would have been obvious to the person of ordinary skill in the art at the time of the invention to

use the round robin scheduler that supplies the data frames to the corresponding transmit port as

taught by Appala et al. with the processor including a split transmit and receive media access

controller having a transmit unit and a receive unit physically separated from one another as

taught by Amit and Stark et al. The round robin scheduler that supplies the data frames to the

corresponding transmit port as taught by Appala et al. can be implemented by coupling the

scheduler to the interface for directing signals between the transmit unit and the receive unit of

the a split transmit and receive media access processor as taught by Amit and Stark et al. The

motivation for using the round robin scheduler that supplies the data frames to the corresponding

transmit port as taught by Appala et al. with the split transmit and receive media access

controller processor as taught by Amit and Stark et al. is to enable prioritized queuing of layer 2

network traffic.

12.   Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Amit (U.S. Patent

7,197,045) in view of Stark et al. (U.S. Patent 6,963,535) and further in view of Wakemen et al.

(U.S. Patent 5,790,786).

For claim 18, Amit discloses a processor comprising at least a portion of a first split

transmit and receive media access controller, the split transmit and receive media access

controller having a transmit unit and a receive unit physically separated from one another *(see*

column 2 lines 28-33, which recite separated MAC receivers and transmitters), wherein the

processor multiplexes onto a common interface signals to be directed between the transmit unit

and the receive unit of the first split transmit and receive media access controller *(column 5 lines*

1-14, which recite a CPU 230 that directs packets between receivers and transmitters),

wherein the multiplexing step further comprises the step of: associating the first and

second split transmit and receive media access controllers with respective distinct addresses

encoded by particular values of information bits sent over the interface; wherein said information

bits are decoded so as to distinguish a first signal sent between the transmit and receive units of

the first split transmit and receive media access controller from a second signal sent between the

transmit and receive units of the second split transmit and receive media access controller *(see*

column 5 lines 1-14, which recite CPU 230 that utilizes information bits to distinguish signals

belonging a first and second transmitter and a second information bit to distinguish signals

belonging a first and second receiver; since each transmitter and receiver is identified by a

unique bit value, each transmit and receive controller can be uniquely identified by specifying

the corresponding receiver and transmitter).

Amit discloses all the subject matter of the claimed invention with the exception wherein

the processor comprises the step of multiplexing onto a common interface signals to be directed

between a transmit unit and a receive unit of at least a second split transmit and receive media

access controller. Stark et al. from the same or similar fields of endeavor teach a MAC bus that

provides connections between a number of MAC interfaces using a multiplexer scheme *(see abstract)*. The MAC bus uses multiplexers that include a MAC data-in bus and MAC data-out bus *(see column 3 lines 19-30)* that allows data from one MAC interface to reach another MAC interface *(see figure 3)*. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the MAC bus that provides connections between a number of MAC interfaces as taught by Stark et al. with the MAC interface that provides separate transmit and receive units as taught by Amit. The MAC bus and multiplexers as taught by Stark et al. can be coupled between the switch interface 352 and each of the receive 336 or transmit 334 MAC interfaces as taught by Amit to provide an interface that is configured to multiplex signals between the transmit unit and the receive unit of the first split transmit and receive media access controller with signals directed between a transmit unit and a receive unit of at least a second split transmit and receive media access controller.The motivation for using the MAC bus interface with the MAC interface that includes separated transmit and receive units is to improve the compatibility of the MAC communication bus with a variety of MAC interfaces.

   Amit and Stark et al. disclose all the subject matter of the claimed invention with the exception wherein the processor includes processor-readable storage medium for use in conjunction with a processor, the medium having embodied therein processor-executable instructions implement the function of the processor. Wakeman et al. from the same or similar fields of endeavor teach a portion of a media access controller including a plurality of receive data path units that are multiplexed to a plurality of transmit data path units *(see column 2 lines 34-46)* that can be implemented by as processor-executable instructions *(see column 11 lines 1-13)*. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the

invention to use plurality of receive data path units are multiplexed with a plurality of transmit

data path units through a bus interface unit implemented by software as taught by Wakeman et

al. with the with the MAC interface that provides separate transmit and receive units as taught by

Amit. The plurality of receive data path units are multiplexed with a plurality of transmit data

path units through a bus interface unit that is implemented by software as taught by Wakeman et

al. can be implemented by replacing the transmit and receive data paths as taught by Wakeman et

al with the MAC interface that provides separate transmit and receive units as taught by Amit.

The motivation for using the plurality of receive data path units are multiplexed with a plurality

of transmit data path units through a bus interface unit that is implemented by software as taught

by Wakeman et al. with the MAC interface that provides separate transmit and receive units as

taught by Amit is to allow greater configurability of the system.

Response to Arguments

13.   It is noted with appreciation that the Applicant has carefully considered the previous

Office Action and the cited prior art references. The Applicant has amended independent claim

1 as follows:

> 1. (Currently amended) A processor comprising:
>   at least a portion of a first split transmit and receive media access
> controller;
>   the split transmit and receive media access controller having a transmit
> unit and a receive unit physically separated from one another;
>   wherein the processor comprises an interface for directing signals between
> the transmit unit and the receive unit of the first split transmit and receive media
> access controller, the interface being configured to multiplex the signals with
> signals directed between a transmit unit and a receive unit of at least a second
> split transmit and receive media access controller;
>   wherein the first and second split transmit and receive media access
> controllers have respective distinct addresses encoded by particular values of

> information bits sent over the interface and the processor decodes said
> information bits so as to distinguish a first signal sent between the transmit and
> receive units of the first split transmit and receive media access controller from a
> second signal sent between the transmit and receive units of the second split
> transmit and receive media access controller.

It is noted that Amit (U.S. Patent 7,197,045) discloses a CPU 230 that directs packets

between the plurality of receivers and transmitters. CPU 230 uses a bit to indicate whether a

packet should be sent to transmitter 1 or transmitter 2. Similarly, CPU 230 uses another bit to

indicate whether a packet is received from receiver 1 or receiver 2 *(see column 5 lines 1-14 and*

figures 4-6). Since each transmitter and receiver is identified by a unique bit value, each transmit

and receive controller can be uniquely identified by CPU 230 using the bits to specify the

corresponding receiver and transmitter. Thus, Amit discloses the first and second split transmit

and receive media access controllers have respective distinct addresses encoded by particular

values of information bits sent over the interface and the processor decodes said information bits

so as to distinguish a first signal sent between the transmit and receive units of the first split

transmit and receive media access controller from a second signal sent between the transmit and

receive units of the second split transmit and receive media access controller as recited by claim

1. Independent claims 17-19 were amended to include similar limitations. They are similarly

rejected under 35 U.S.C. 103(a) as being unpatentable over Amit (U.S. Patent 7,197,045) in view

of Stark et al. (U.S. Patent 6,963,535).

Conclusion

14.   Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this

final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to BEN H. LIU whose telephone number is (571)270-3118. The

examiner can normally be reached on 9:00AM to 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Ricky Ngo can be reached on (571)272-3139. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ricky Ngo/
Supervisory Patent Examiner, Art Unit
2416

BL